CLAIMS

What is claimed is:

1. A register file comprising:

   a local bit trace;

   a driving signal trace;

   a plurality of data cells coupled to the local bit trace; and

   a device coupled to the driving signal trace and the local bit trace to intelligently charge and float the local bit trace, the intelligent charging and floating facilitated by determination of a selection of one of the data cells.

2. The register file of claim 1 wherein the intelligent charging and floating comprises selectively coupling and decoupling the driving signal trace and the local bit trace to and from each other, including decoupling the driving signal trace from the local bit trace when one of the data cells is selected.

3. The register file of claim 1 wherein the device comprises at least one interruptible inverting logic stage and wherein an input of the interruptible inverting logic stage is coupled to the driving signal trace and wherein an output of the inverting logic stage is coupled to the local bit trace.

4. The register file of claim 1 wherein the driving signal trace comprises a power supply trace.

5. The register file of claim 4 wherein the device comprises a PMOS transistor and wherein a drain of the PMOS transistor is coupled to the driving signal trace and a source of the PMOS transistor is coupled to the local bit trace.

6. The register file of claim 1 further comprising first decode logic coupled to the device to signal the device on the selection of one of the data cells.

7. The register file of claim 6 further comprising a plurality of address signal traces coupled to the first decode logic, which determines the selection of one of the data cells based on a first subset of the plurality of address signal traces.

8. The register file of claim 7 wherein the first subset of the plurality of address signal traces include one or more most significant bits of the address signal traces.

9. The register file of claim 1 further comprising a plurality of low threshold voltage transistors to couple the plurality of data cells to the local bit trace.

10. The register file of claim 10 further comprising second decode logic coupled to the low threshold voltage transistors to provide the transistors with read enable signals based at least in part on the second decode logic's decoding of a second subset of the address signal traces.

11. A register file comprising:

a first and a second local bit trace;

a first and a second driving signal trace;

a plurality of data cells wherein a first subset of the plurality of data cells is coupled to the first local bit trace and a second subset of the plurality of data cells is coupled to the second local bit trace;

a first device coupled to the first driving signal trace and the first local bit trace and a second device coupled to the second driving signal trace

and the second local bit trace, the first and second devices to intelligently charge and float the respective first and second local bit traces, the intelligent charging and floating facilitated by determination of a selection of one of the data cells in the plurality of data cells; and

global multiplexing logic coupled to the first and second local bit traces to facilitate provision of a selected data value of the address data cell on an output signal trace.

12. The register file of claim 11 wherein the intelligent charging and floating comprises selectively coupling and decoupling the respective driving signal trace and the respective local bit trace to and from each other, including decoupling the first driving signal trace from the first local bit trace and coupling the second driving signal trace to the second local bit trace when the addressed data cell is a data cell from the first subset of the plurality of data cells.

13. The register file of claim 11 wherein at least one of the first device and the second device comprises at least one interruptible inverting logic stage and wherein an input of the interruptible inverting logic stage is coupled to the respective driving signal trace and wherein an output of the inverting logic stage is coupled to the respective local bit trace.

14. The register file of claim 11 wherein at least one of the first device and the second device comprises a PMOS transistor and wherein a drain of the PMOS transistor is coupled to the respective driving signal trace and a source of the PMOS transistor is coupled to the respective local bit trace.

15. The register file of claim 11 further comprising first and second decode logic coupled to the first and second device respectively, the first and second decode logic to signal the respective device on the selection of one of the data cells.

16. The register file of claim 15 further comprising a plurality of address signal traces coupled to the first and second decode logic, which determines the selection of one of the data cells based on a first subset of the plurality of address signal traces.

17. The register file of claim 16 further wherein the first subset of the plurality of address signal traces include one or more most significant bits of the address signal traces.

18. The register file of claim 11 further comprising a first and second plurality of low threshold voltage transistors to respectively couple the first and second subset of plurality of data cells to the first and second local bit traces respectively.

19. The register file of claim 18 further comprising third and forth decode logic coupled to the first and second plurality of low threshold voltage transistors to provide the transistors with read enable signals based at least in part on the third and forth decode logic's decoding of a second subset of the address signal traces.

20. A method comprising:

determining whether a set of data cells comprises a selected data cell; and

conditionally electrically decoupling a driving signal trace from a local bit trace upon said determining, said local bit trace coupled to said set of data cells.

21. The method of claim 20 wherein said determining comprises decoding a first subset of address bits.

22. The method of claim 21 wherein said first subset of address bits comprises one or more most significant bits of a set of address bits.

23. A system comprising:

a processor including;

a register file comprising:

a first and a second local bit trace;

a first and a second driving signal trace;

a plurality of data cells wherein a first subset of the plurality of data cells is coupled to the first local bit trace and a second subset of the plurality of data cells is coupled to the second local bit trace;

a first device coupled to the first driving signal trace and the first local bit trace and a second device coupled to the second driving signal trace and the second local bit trace, the first and second devices to intelligently charge and float the respective first and second local bit traces, the intelligent charging and floating facilitated by determination of a selection of one of the data cells in the plurality of data cells; and

global multiplexing logic coupled to the first and second local bit traces to facilitate provision of a selected data value of the address data cell on an output signal trace;

a memory configured to store data; and

a bus coupled to the processor and memory to facilitate data exchange between the processor and memory.

24. The system of claim 23 wherein the intelligent charging and floating comprises selectively coupling and decoupling the respective driving signal trace and the respective local bit trace to and from each other, including decoupling the first driving signal trace from the first local bit trace and coupling the second driving signal trace to the second local bit trace when the addressed data cell is a data cell from the first subset of the plurality of data cells.

25. The system of claim 23 wherein at least one of the first device and the second device comprises at least one interruptible inverting logic stage and wherein an input of the interruptible inverting logic stage is coupled to the respective driving signal trace and wherein an output of the inverting logic stage is coupled to the respective local bit trace.

26. The system of claim 23 wherein at least one of the first device and the second device comprises a PMOS transistor and wherein a drain of the PMOS transistor is coupled to the respective driving signal trace and a source of the PMOS transistor is coupled to the respective local bit trace.

27. The system of claim 23 wherein the register file further comprises first and second decode logic coupled to the first and second device respectively, the first and second decode logic to signal the respective device on the selection of one of the data cells.

28. The system of claim 27 wherein the register file further comprises a plurality of address signal traces coupled to the first and second decode logic, which determines the selection of one of the data cells based on a first subset of the plurality of address signal traces.

29. The system of claim 28 wherein the first subset of the plurality of address signal traces includes one or more most significant bits of the address signal traces.

30. The system of claim 23 wherein the register file further comprises a first and second plurality of low threshold voltage transistors to respectively couple the first and second subset of plurality of data cells to the first and second local bit traces respectively.